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(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD, CIRCUIT BOARD, AND ELECTRIC APPARATUS

(57) A depression (22) is formed from a first surface (20) of a semiconductor substrate (10). An insulating layer (28) is provided on the bottom surface and an inner wall surface of the depression (22). A conductive portion (30) is provided inside the insulating layer (28). A second surface (38) of the semiconductor substrate (10) is etched by a first etchant having characteristics such that the etching amount with respect to the semiconductor substrate (10) is greater than the etching amount with respect to the insulating layer (28), and the conductive portion (30) is caused to project while covered by the insulating layer (28). At least a portion of the insulating layer (28) formed on the bottom surface of the depression (22) is etched with a second etchant having characteristics such that at least the insulating layer (28) is etched without forming a residue on the conductive portion (30), to expose the conductive portion (30).

FIG. 3 A

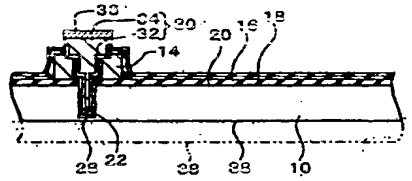


FIG. 3 B

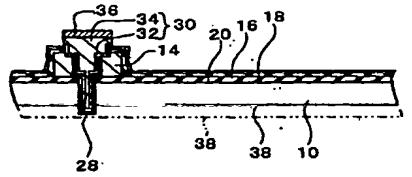
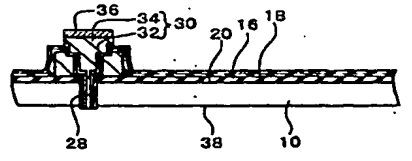


FIG. 3 C



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Description

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device and method of manufacturing the same, a circuit board, and an electronic instrument.

BACKGROUND ART

[0002] A semiconductor device for three-dimensional mounting has been developed. It is known to form electrodes penetrating a semiconductor chip, to enable three-dimensional mounting. The penetrating electrodes are formed to project from the semiconductor chip. In the conventionally known method of forming a penetrating electrode, a portion of silicon around the penetrating electrode is etched, whereby the penetrating electrode is caused to project. In this case, it is difficult to prevent the projecting portion of the penetrating electrode from being contaminated by the etching gas.

DISCLOSURE OF THE INVENTION

[0003] The present invention solves the existing problems, and has as its object the formation of a penetrating electrode of high quality.

(1) According to one aspect of the present invention, there is provided a method of manufacturing a semiconductor device comprising:

(a) forming a depression from a first surface of a semiconductor substrate in which an integrated circuit is formed;
(b) providing an insulating layer on the bottom surface and an inner wall surface of the depression;
(c) providing a conductive portion inside the insulating layer;
(d) etching a second surface of the semiconductor substrate opposite to the first surface, with a first etchant having characteristics such that the etching amount with respect to the semiconductor substrate is greater than the etching amount with respect to the insulating layer, to cause the conductive portion to project while covered by the insulating layer;
(e) etching at least a portion of the insulating layer formed on the bottom surface of the depression with a second etchant having characteristics such that at least the insulating layer is etched without forming a residue on the conductive portion, to expose the conductive portion. According to this aspect of the present invention, the conductive portion is caused to project in the step (d), and the conductive portion is exposed in the step (e). In this way, a penetrating electrode projecting from the semiconductor substrate can be formed from the conductive portion. In the step (e), when the conductive portion is exposed from the insulating layer, no residues are left on the conductive portion, and therefore a penetrating electrode of high quality can be formed.

(2) In this method of manufacturing a semiconductor device,

the first etchant may be one of SF_6, CF_4, and Cl_2 gases.

(3) In this method of manufacturing a semiconductor device,

the step (d) may be carried out using a dry etching device.

(4) In this method of manufacturing a semiconductor device,

the first etchant may be one of a liquid mixture of hydrofluoric acid and nitric acid, and a liquid mixture of hydrofluoric acid, nitric acid, and acetic acid.

(5) In this method of manufacturing a semiconductor device,

the second etchant may be one of a gas mixture of argon and CF_4, and a gas mixture of O_2 and CF_4.

(6) In this method of manufacturing a semiconductor device,

the step (e) may be carried out using a dry etching device.

(7) In this method of manufacturing a semiconductor device,

the second etchant may be one of liquid hydrofluoric acid, and a liquid mixture of hydrofluoric acid and ammonium fluoride.

(8) In this method of manufacturing a semiconductor device,

the insulating layer may be formed of one of SiO_2 and SiN.

(9) In this method of manufacturing a semiconductor device,

an outer layer of the conductive portion may also be etched in the step (e).

(10) In this method of manufacturing a semiconductor device,

the outer layer and a central portion of the conductive portion may be formed of different materials.

(11) In this method of manufacturing a semiconductor device,

the central portion of the conductive portion may be formed of one of copper, tungsten, and doped polysilicon.

(12) In this method of manufacturing a semiconductor device,

at least a part of the outer layer of the conductive portion may be formed of one of TiW, TiN, and TaN.

(13) This method of manufacturing a semiconductor device may further comprise,

polishing the second surface of the semiconductor substrate up to a point before the insulating layer before the step (d)

(14) In this method of manufacturing a semiconductor device,

the etching of the step (e) may have a lower etching rate with respect to the semiconductor substrate than the etching of the step (d).

(15) In this method of manufacturing a semiconductor device,

the semiconductor substrate may be a semiconductor wafer having a plurality of the integrated circuits, the depression being formed for each of the integrated circuits,

the method further comprising cutting the semiconductor substrate.

(16) In this method of manufacturing a semiconductor device,

the step of cutting the semiconductor substrate may comprise:

forming a groove in the first surface, along a cutting line of the semiconductor substrate; and removing a bottom portion of the groove from the second surface so that the groove becomes a slit.

(17) In this method of manufacturing a semiconductor device,

the groove may be formed by cutting.

(18) In this method of manufacturing a semiconductor device,

the groove may be formed by etching.

(19) In this method of manufacturing a semiconductor device,

the groove may be formed in the same process as the depression in the step (a).

(20) In this method of manufacturing a semiconductor device,

the groove may be formed to be deeper than the depression; and

a bottom portion of the groove may be removed by the polishing of the second surface of the semiconductor substrate.

(21) In this method of manufacturing a semiconductor device,

the insulating layer may be provided also within the groove in the step (b).

(22) In this method of manufacturing a semiconductor device,

part of the insulating layer formed on a bottom portion of the groove may be caused to project from the second surface in the step (d); and

the part of the insulating layer formed on a bottom portion of the groove may be etched and removed by means of the second etchant in the step (e).

(23) In this method of manufacturing a semiconductor device,

the step of removing the bottom portion of the groove may be carried out in a state that a material of the semiconductor substrate is exposed within the groove.

(24) In this method of manufacturing a semiconductor device,

the bottom portion of the groove formed by a part of the semiconductor substrate may be etched and removed by means of the first etchant in the step (d).

(25) In this method of manufacturing a semiconductor device,

the step of cutting the semiconductor substrate may be carried out with a protective sheet adhered to the first surface of the semiconductor substrate, so that a plurality of semiconductor chips obtained by cutting do not fall apart.

(26) In this method of manufacturing a semiconductor device,

the groove may be formed only in regions sectioning the semiconductor substrate into a plurality of semiconductor chips having the plurality of integrated circuits.

(27) According to another aspect of the present invention, there is provided a method of manufacturing a semiconductor device, comprising:

laminating a plurality of semiconductor devices manufactured by the above described method; and

making electrical connections between the semiconductor devices through the conductive portions.

(28) According to further aspect of the present invention, there is provided a semiconductor device manufactured by the above described method.

(29) According to still another aspect of the present invention, there is provided a circuit board on which is mounted the above described semiconductor device.

(30) According to still further aspect of the present invention, there is provided an electronic instrument having the above described semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004]

Figs. 1A to 1D are diagrams for illustrating a method of manufacturing a semiconductor device according to a first embodiment of the present invention.

Figs. 2A to 2D are diagrams for illustrating the method of manufacturing a semiconductor device according to the first embodiment of the present in-

vention.

Figs. 3A to 3C are diagrams for illustrating the method of manufacturing a semiconductor device according to the first embodiment of the present invention.

Fig. 4 is a diagram for illustrating the method of manufacturing a semiconductor device according to the first embodiment of the present invention.

Fig. 5 is a diagram for illustrating the method of manufacturing a semiconductor device according to the first embodiment of the present invention.

Fig. 6 is a diagram showing a circuit board according to the first embodiment of the present invention.

Fig. 7 is a diagram showing an electronic instrument according to the first embodiment of the present invention.

Fig. 8 is a diagram showing an electronic instrument according to the first embodiment of the present invention.

Figs. 9A to 9C are diagrams for illustrating a method of manufacturing a semiconductor device according to a second embodiment of the present invention.

Figs. 10A and 10B are diagrams for illustrating a method of manufacturing a semiconductor device according to a third embodiment of the present invention.

Figs. 11 A and 11B are diagrams for illustrating a method of manufacturing a semiconductor device according to a fourth embodiment of the present invention.

Fig. 12 is a diagram for illustrating a method of manufacturing a semiconductor device according to a fifth embodiment of the present invention.

Fig. 13 is a diagram for illustrating a method of manufacturing a semiconductor device according to a sixth embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0005] Embodiments of the present invention are now described with reference to the drawings.

First Embodiment

[0006] Figs. 1A to 3C are diagrams for illustrating a method of manufacturing a semiconductor device according to a first embodiment of the present invention. In this embodiment, a semiconductor substrate 10 is used. The semiconductor substrate 10 shown in Fig. 1A is a semiconductor wafer, but it may be a semiconductor chip. On the semiconductor substrate 10 is formed at least one (a plurality on a semiconductor wafer; one on a semiconductor chip) integrated circuit (for example, a circuit comprising transistors or memory) 12. On the semiconductor substrate 10 are formed a plurality of electrodes (for example, pads) 14. Each electrode 14 is electrically connected to the integrated circuit 12. The electrodes 14 may be formed of aluminum. The surface form of the electrodes 14 is not particularly restricted, but is commonly rectangular. When the semiconductor substrate 10 is a semiconductor wafer, in each of the regions for the plurality of semiconductor chips, two or more (one group of) electrodes 14 are formed.

[0007] On the semiconductor substrate 10 are formed passivation films 16 and 18, of a single layer or more layers. The passivation films 16 and 18 can be formed of, for example, SiO_2, SiN, polyimide resin, or the like. In the example shown in Fig. 1A, on the passivation film 16, the electrodes 14, and interconnecting lines (not shown in the drawings) connecting the integrated circuit 12 and electrodes 14 are formed. The other passivation film 18 is formed so as to avoid at least a part of the surface of the electrodes 14. After forming the passivation film 18 to cover the surface of the electrodes 14, a part may be etched to expose a part of the electrodes 14. For the etching, either dry etching or wet etching may be applied. When etching the passivation film 18, the surface of the electrodes 14 may be etched.

[0008] In this embodiment, in the semiconductor substrate 10, a depression 22 (see Fig. 1C) is formed from a first surface 20 thereof. The first surface 20 is the surface on which the electrodes 14 are formed. The depression 22 is formed to avoid the elements and interconnecting lines of the integrated circuit 12. As shown in Fig. 1B, a through hole 24 may be formed in the electrodes 14. To form the through hole 24, etching (dry etching or wet etching) may be applied. The etching may be carried out after using a lithography process to form a patterned resist (not shown in the drawings). When the passivation film 16 is formed beneath the electrodes 14, a through hole 26 (see Fig. 1C) is also formed therein. When the etching of the electrodes 14 is stopped by the passivation film 16, for the formation of the through hole 26 the etchant used for etching the electrodes 14 may be replaced by a different etchant. In this case, once again, a patterned resist (not shown in the drawings) may be formed by a lithography process.

[0009] As shown in Fig. 1C, the depression 22 is formed in the semiconductor substrate 10 so as to communicate with the through hole 24 (and through hole 26). The through hole 24 (and through hole 26) and depression 22 can also be referred to collectively as a depression. For the formation of the depression 22, etching (dry etching or wet etching) can be applied. Etching may be carried out after forming a patterned resist (not shown in the drawings) by a lithography process. Alternatively, for the formation of the depression 22, a laser (for example, a CO_2 laser, a YAG laser, or the like) may be used. The laser may be applied to the formation of the through holes 24 and 26. The depression 22 and through holes 24 and 26 may also be formed together by the use of a single etchant or laser.

[0010] As shown in Fig. 1D, on the inner surface of the depression 22, an insulating layer 28 is formed. The insulating layer 28 may be an oxidation film. For exam-

ple, if the material of the semiconductor substrate 10 is silicon, the insulating layer 28 may be of SiO_2 or SiN. The insulating layer 28 is formed on the bottom surface of the depression 22. The insulating layer 28 is formed on the inner wall of the depression 22. However, the insulating layer 28 is formed so as not to fill in the depression 22. That is to say, a depression is formed by the insulating layer 28. The insulating layer 28 may be formed on the inner wall of the through hole 26 in the passivation film 16. The insulating layer 28 may be formed over the passivation film 18.

[0011] The insulating layer 28 may be formed on the inner wall of the through hole 24 in the electrodes 14. The insulating layer 28 is formed to avoid a part of the electrodes 14 (for example, the top surface thereof). The insulating layer 28 may be formed to cover the whole surface of the electrodes 14, and then by partial etching (dry etching or wet etching), a part of the electrodes 14 exposed. The etching may be carried out after forming a patterned resist (not shown in the drawings) by a lithography process.

[0012] Next, a conductive portion 30 (see Fig. 2B) is provided inside the insulating layer 28. The conductive portion 30 may be formed of copper, tungsten, or the like. As shown in Fig. 2A, after an outer layer 32 of the conductive portion 30 is formed, a central portion 34 thereof may be formed. The central portion 34 can be formed of any of copper, tungsten, or doped polysilicon (for example, low temperature polysilicon). The outer layer 32 may include at least a barrier layer. The barrier layer prevents the material of the central portion 34 or of the seed layer described next from diffusing into the semiconductor substrate 10 (for example silicon). The barrier layer may be formed of a different material from the central portion 34 (for example, TiW, TiN, or TaN). If the central portion 34 is formed by electroplating, the outer layer 32 may include a seed layer. The seed layer is formed after forming the barrier layer. The seed layer is formed of the same material (for example copper) as the central portion 34. It should be noted that the conductive portion 30 (at least the central portion 34 thereof) may be formed by electroless plating or an inkjet method.

[0013] As shown in Fig. 2B, when the outer layer 32 is also formed over the passivation film 18, as shown in Fig. 2C, the part of the outer layer 32 over the passivation film 18 is etched. By forming the central portion 34 after the outer layer 32 is formed, the conductive portion 30 can be provided. A part of the conductive portion 30 is positioned within the depression 22 in the semiconductor substrate 10. Between the inner surface of the depression 22 and the conductive portion 30 is interposed the insulating layer 28, and therefore the two are electrically isolated. The conductive portion 30 is electrically connected to the electrodes 14. For example, a portion of the electrodes 14 exposed from the insulating layer 28 may contact the conductive portion 30. A part of the conductive portion 30 may be positioned over the passivation film 18. The conductive portion 30 may be provided only within the region of the electrodes 14. The conductive portion 30 may project, at least above the depression 22. For example, the conductive portion 30 may project from the passivation film 18.

[0014] It should be noted that as a variant, the central portion 34 may be formed with the outer layer 32 remaining on the passivation film 18. In that case, since a layer continuous with the central portion 34 is also formed over the passivation film 18, this layer is etched.

[0015] As shown in Fig. 2D, over the conductive portion 30, a brazing material layer 36 may be provided. The brazing material layer 36 is formed, for example, of solder, and may be formed of either of soft solder or hard solder. The brazing material layer 36 may be formed by covering regions other than the second conductive portion 32 with a resist. By the above process, bumps can be formed by the conductive portion 30 or with the addition of the brazing material layer 36.

[0016] In this embodiment, as shown in Fig. 3A, a second surface of the semiconductor substrate 10 (the surface on the opposite side to the first surface 20) may be removed by, for example, at least one of mechanical polishing or grinding and chemical polishing or grinding. This process is carried out up to a point before the insulating layer 28 formed in the depression 22 is exposed. It should be noted that the process shown in Fig. 3A may be omitted, and next the process of Fig. 3B carried out.

[0017] As shown in Fig. 3B, the second surface 38 of the semiconductor substrate 10 is etched so that the insulating layer 28 is exposed. The second surface 38 of the semiconductor substrate 10 is etched so that the conductive portion 30 (more precisely, the portion within the depression 22 thereof) projects while covered by the insulating layer 28. The etching is carried out with a first etchant, whose properties are such as to yield a greater etching amount with respect to the semiconductor substrate (for example, a silicon base material) 10 than with respect to the insulating layer (for example, formed of SiO_2) 28. The first etchant may be SF_6, CF_4, or Cl_2 gas. The etching may be carried out using a dry etching device. Alternatively, the first etchant may be a mixture of hydrofluoric acid and nitric acid, or a mixture of hydrofluoric acid, nitric acid, and acetic acid.

[0018] As shown in Fig. 3C, at least the portion of the insulating layer 28 formed on the bottom surface of the depression 22 is etched. Then the conductive portion 30 is exposed. The extreme surface of the conductive portion 30 may be exposed, and the peripheral surface of the extremity of the conductive portion 30 covered by the insulating layer 28. The outer layer 32 (for example, a barrier layer) of the conductive portion 30 may also be etched. The etching is carried out with a second etchant of characteristics such as to etch at least the insulating layer 28 without forming residues on the conductive portion 30. For the second etchant may be used an etchant which does not react (or has little reaction) with the ma-

terial (for example, copper) of the conductive portion 30. The second etchant may be a mixture of argon and CF_4 gas, or a mixture of O_2 and CF_4 gas. The etching may be carried out using a dry etching device. Alternatively, the second etchant may be liquid hydrofluoric acid, or a liquid mixture of hydrofluoric acid and ammonium fluoride. The etching by the second etchant may have an etching rate with respect to the semiconductor substrate 10 which is slower than etching by the first etchant.

[0019] It should be noted that in at least one step in Figs. 3A to 3C, a reinforcing member of, for example, resin layer or resin tape may be provided on the first surface 20 of the semiconductor substrate 10.

[0020] By the above process, the conductive portion 30 can be caused to project from the second surface 38 of the semiconductor substrate 10. The projecting conductive portion 30 forms a projecting electrode. The conductive portion 30 also forms penetrating electrodes of the first and second surfaces 20 and 38. According to this embodiment, when exposing the conductive portion 30 from the insulating layer 28, since no residues are left on the conductive portion 30, penetrating electrodes of high quality can be formed.

[0021] As shown in Fig. 4, when the semiconductor substrate 10 is a semiconductor wafer, concavities 22 may be formed corresponding to individual integrated circuits 12 (See Fig. 1A), and the semiconductor substrate 10 may be cut (for example, by dicing). For the cutting, a cutter (for example, a dicer) 40 or laser (for example, a CO_2 laser, YAG laser, or the like) may be used.

[0022] By the above process, a semiconductor device can be manufactured. As shown in Fig. 5, a plurality of semiconductor devices manufactured by the above described method may be laminated, and electrical connection therebetween may be achieved through respective conductive portions 30. This embodiment is effective for carrying out such a three-dimensional mounting. The semiconductor device shown in Fig. 5 has a plurality of semiconductor substrates 10. In the direction of the first surface 20, the outermost positioned (in Fig. 5, the lowest) semiconductor substrate 10 has external terminals (for example, solder balls) 42. The external terminals 42 are provided, on interconnecting lines 46 formed over a resin layer (for example, a stress relieving layer) 44. The interconnecting lines 46 are connected to the conductive portion 30 on the first surface 20.

[0023] In Fig. 6 is shown a circuit board 1000 on which is mounted a semiconductor device 1, formed of a laminated plurality of semiconductor chips. The plurality of semiconductor chips is electrically connected by the above described conductive portion 30. As an electronic instrument having the above described semiconductor device, Fig. 7 shows a notebook personal computer 2000, and Fig. 8 shows a mobile telephone 3000.

Second Embodiment

[0024] Figs. 9A to 9C are diagrams for illustrating a method of manufacturing a semiconductor device according to a second embodiment of the present invention. In this embodiment, a groove 100 is formed in the semiconductor substrate 10 (more precisely, in the first surface 20 thereof). The groove 100 is formed along the cutting line of the semiconductor substrate 10. The groove 100 may be formed by cutting, or may be formed by etching. The groove 100 may be formed in the step of forming the depression 22 shown in Fig. 1C, with the same process (for example, at the same time) as the depression 22. The insulating layer 28 may be provided within the groove 100. The groove 100 may be of substantially the same depth as the depression 22, or may be deeper than the depression 22, or may be shallower than the depression 22.

[0025] Thereafter, the process described in Figs. 3A to 3C in the first embodiment is carried out. Figs. 9A to 9C show the configuration in the vicinity of the groove 100 when the respective steps shown in Figs. 3A to 3C are carried out. For example, the process shown in Fig. 3A is carried out, and the second surface 38 of the semiconductor substrate 10 is polished to a point short of the insulating layer 28 (see Fig. 9A). The process shown in Fig. 3B is carried out, as shown in Fig. 9B, and the insulating layer 28 formed at the bottom of the groove 100 is caused to project from the second surface 38.

[0026] Then, the process shown in Fig. 3C is carried out, as shown in Fig. 9C, and by means of the second etchant, the insulating layer 28 formed at the bottom of the groove 100 is etched and removed. In this way, the bottom portion of the groove 100 is removed from the second surface, and the groove 100 becomes a slit 102. That is to say, the semiconductor substrate 100 is cut along the groove 100.

[0027] According to this embodiment, the semiconductor substrate 10 can be cut simply. Since final cutting of the semiconductor substrate 10 is carried out by means of the second etchant, chipping is not likely to occur. Furthermore, in this embodiment, since the insulating layer 28 is formed within the groove 100, the semiconductor chip has the insulating layer 28 on the edge surface. Therefore, this semiconductor chip is not susceptible to edge shorting. Other details are as described in the first embodiment.

Third Embodiment

[0028] Figs. 10A and 10B are diagrams for illustrating a method of manufacturing a semiconductor device according to a third embodiment of the present invention. In this embodiment, as shown in Fig. 10A, the process of removing the bottom portion of the groove 100 is carried out with the material of the semiconductor substrate 10 exposed within the groove 100. For example, after carrying out the process of forming the insulating layer

28 shown in Fig. 1D within the depression 22, the groove 100 may be formed, and in order that the insulating layer 28 is not attached, a resist or the like may be provided within the groove 100, or the insulating layer 28 which has entered the groove 100 may be removed. Other details are as described in the second embodiment.

[0029] In this embodiment, the process of Fig. 3B described in the first embodiment is carried out, and by means of the first etchant, the bottom portion of the groove 100 formed by a part of the semiconductor substrate 10 is etched and removed. In this way, as shown in Fig. 10B, the bottom portion of the groove 100 is removed from the second surface, and the groove 100 becomes the slit 102. That is to say, the semiconductor substrate 100 is cut along the groove 100. Other details are as described in the first and second embodiments.

Fourth Embodiment

[0030] Figs. 11A and 11B are diagrams for illustrating a method of manufacturing a semiconductor device according to a fourth embodiment of the present invention. In this embodiment, as shown in Fig. 11A, a groove 110 is formed to be deeper than the depression 22. The groove 110 deeper than the depression 22 can be formed easily, exploiting the etching characteristics (the property of etching deeper in a wider spaces).

[0031] Then as shown in Fig. Fig. 11B, by polishing the second surface 38 of the semiconductor substrate 10 (refer to the description relating to Fig. 3A), the bottom portion of the groove 110 is removed. In this way, the bottom portion of the groove 110 is removed from the second surface, and the groove 110 becomes a slit 112. That is to say, the semiconductor substrate 100 is cut along the groove 110. Other details are as described in the first, second, and third embodiments. In this embodiment, the semiconductor substrate 10 is cut while the insulating layer 28 is formed within the groove 110, but the semiconductor substrate 10 may equally be cut while the material of the semiconductor substrate 10 is exposed within the groove 110.

Fifth Embodiment

[0032] Fig. 12 is a diagram for illustrating a method of manufacturing a semiconductor device according to a fifth embodiment of the present invention. The content of this embodiment can be applied to any from the second to the fourth embodiments. In this embodiment, a groove 120 is formed only in regions delineating a plurality of semiconductor chips having a plurality of integrated circuits 12 (See Fig. 1A). By this means, parts of the semiconductor substrate 10 that are not needed (for example, an outer peripheral portion) do not become separated, and damage to the semiconductor chip forming the product can be prevented.

Sixth Embodiment

[0033] Fig. 13 is a diagram for illustrating a method of manufacturing a semiconductor device according to a sixth embodiment of the present invention. In this embodiment, the step of cutting the semiconductor substrate 10 is carried out after attaching a protective sheet 130 to the first surface 20 of the semiconductor substrate 10. The protective sheet 130 may be an adhesive tape or adhesive sheet. By means of this, even when the semiconductor substrate 10 is cut, the plurality of semiconductor chips does not fall apart. The content of this embodiment can be applied to any from the first to the fifth embodiments.

[0034] The present invention is not limited to the above-described embodiments, and various modifications can be made. For example, the present invention includes various other configurations substantially the same as the configurations described in the embodiments (in function, method and effect, or in objective and effect, for example). The present invention also includes a configuration in which an unsubstantial portion in the described embodiments is replaced. The present invention also includes a configuration having the same effects as the configurations described in the embodiments, or a configuration able to achieve the same objective. Further, the present invention includes a configuration in which a publicly known technique is added to the configurations in the embodiments.

Claims

1. A method of manufacturing a semiconductor device comprising:

   (a) forming a depression from a first surface of a semiconductor substrate in which an integrated circuit is formed;
   (b) providing an insulating layer on the bottom surface and an inner wall surface of the depression;
   (c) providing a conductive portion inside the insulating layer;
   (d) etching a second surface of the semiconductor substrate opposite to the first surface, with a first etchant having characteristics such that the etching amount with respect to the semiconductor substrate is greater than the etching amount with respect to the insulating layer, to cause the conductive portion to project while covered by the insulating layer;
   (e) etching at least a portion of the insulating layer formed on the bottom surface of the depression with a second etchant having characteristics such that at least the insulating layer is etched without forming a residue on the conductive portion, to expose the conductive por-

tion.

2. The method as defined in claim 1, wherein the first etchant is one of SF_6, CF_4, and Cl_2 gases.

3. The method as defined in claim 2, wherein the step (d) is carried out using a dry etching device.

4. The method as defined in claim 1, wherein the first etchant is one of a liquid mixture of hydrofluoric acid and nitric acid, and a liquid mixture of hydrofluoric acid, nitric acid, and acetic acid.

5. The method as defined in claim 1, wherein the second etchant is one of a gas mixture of argon and CF_4, and a gas mixture of O_2 and CF_4.

6. The method as defined in claim 5, wherein the step (e) is carried out using a dry etching device.

7. The method as defined in claim 1, wherein the second etchant is one of liquid hydrofluoric acid, and a liquid mixture of hydrofluoric acid and ammonium fluoride.

8. The method as defined in claim 1, wherein the insulating layer is formed of one of SiO_2 and SiN.

9. The method as defined in claim 1, wherein an outer layer of the conductive portion is also etched in the step (e).

10. The method as defined in claim 9, wherein the outer layer and a central portion of the conductive portion are formed of different materials.

11. The method as defined in claim 10, wherein the central portion of the conductive portion is formed of one of copper, tungsten, and doped polysilicon.

12. The method as defined in claim 10, wherein at least a part of the outer layer of the conductive portion is formed of one of TiW, TiN, and TaN.

13. The method as defined in claim 1, further comprising:

polishing the second surface of the semiconductor substrate up to a point before the insulating layer before the step (d).

14. The method as defined in claim 1, wherein the etching of the step (e) has a lower etching rate with respect to the semiconductor substrate than the etching of the step (d).

15. The method as defined in claim 1, wherein the semiconductor substrate is a semiconductor wafer having a plurality of the integrated circuits, the depression being formed for each of the integrated circuits,

the method further comprising cutting the semiconductor substrate.

16. The method as defined in claim 15, wherein the step of cutting the semiconductor substrate comprises:

forming a groove in the first surface, along a cutting line of the semiconductor substrate; and removing a bottom portion of the groove from the second surface so that the groove becomes a slit.

17. The method as defined in claim 16, wherein the groove is formed by cutting.

18. The method as defined in claim 16, wherein the groove is formed by etching.

19. The method as defined in claim 16, wherein the groove is formed in the same process as the depression in the step (a).

20. The method as defined in claim 16, further comprising:

polishing the second surface of the semiconductor substrate up to a point before the insulating layer before the step (d),

wherein the groove is formed to be deeper than the depression; and

wherein a bottom portion of the groove is removed by the polishing of the second surface of the semiconductor substrate.

21. The method as defined in claim 16, wherein the insulating layer is provided also within the groove in the step (b).

22. The method as defined in claim 21, wherein part of the insulating layer formed on a bottom portion of the groove is caused to project from the second surface in the step (d); and

wherein the part of the insulating layer formed on a bottom portion of the groove is etched and re-

moved by means of the second etchant in the step (e).

23. The method as defined in claim 16, wherein the step of removing the bottom portion of the groove is carried out in a state that a material of the semiconductor substrate is exposed within the groove.

24. The method as defined in claim 23, wherein the bottom portion of the groove formed by a part of the semiconductor substrate is etched and removed by means of the first etchant in the step (d).

25. The method as defined in claim 16, wherein the step of cutting the semiconductor substrate is carried out with a protective sheet adhered to the first surface of the semiconductor substrate, so that a plurality of semiconductor chips obtained by cutting do not fall apart.

26. The method as defined in claim 16, wherein the groove is formed only in regions sectioning the semiconductor substrate into a plurality of semiconductor chips having the plurality of integrated circuits.

27. A method of manufacturing a semiconductor device, comprising:

laminating a plurality of semiconductor devices manufactured by the method as defined in any one of claims 1 to 26; and
making electrical connections between the semiconductor devices through the conductive portions.

28. A semiconductor device manufactured by the method as defined in any one of claims 1 to 26.

29. A semiconductor device manufactured by the method as defined in claim 27.

30. A circuit board on which is mounted the semiconductor device as defined in claim 28.

31. A circuit board on which is mounted the semiconductor device as defined in claim 29.

32. An electronic instrument having the semiconductor device as defined in claim 28.

33. An electronic instrument having the semiconductor device as defined in claim 29.

FIG. 1 A

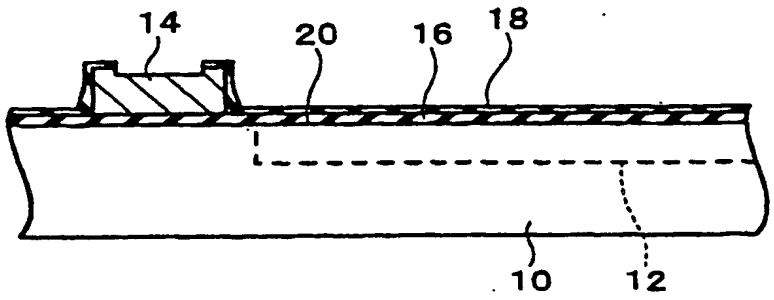


FIG. 1 B

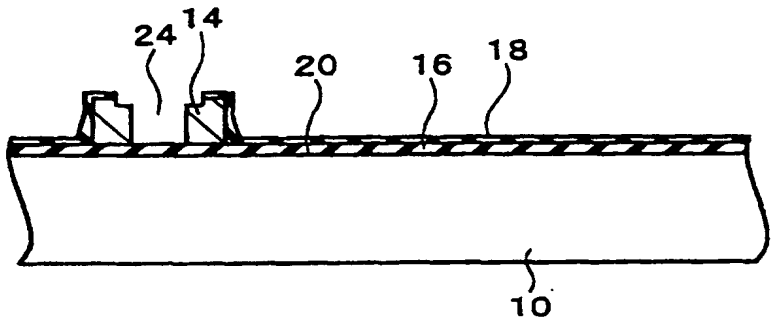


FIG. 1 C

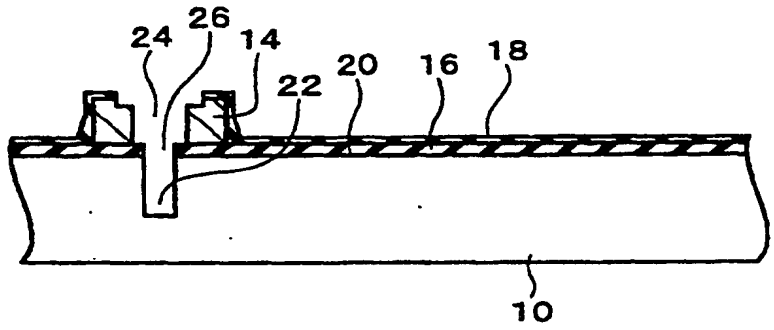


FIG. 1 D

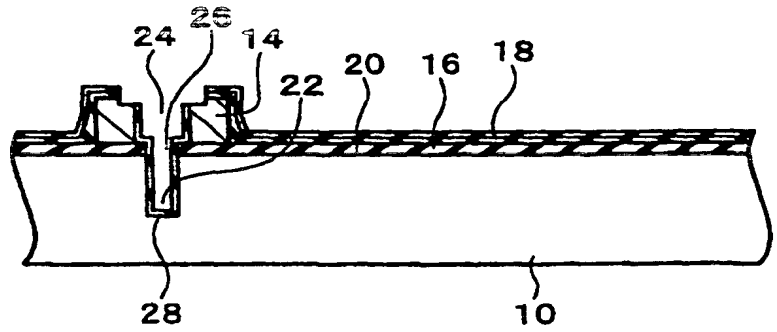


FIG. 2 A

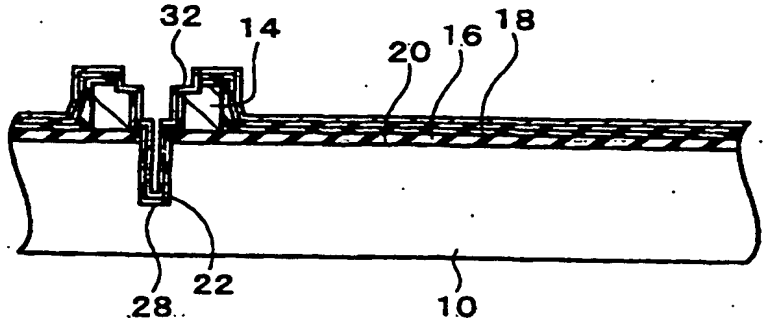


FIG. 2 B

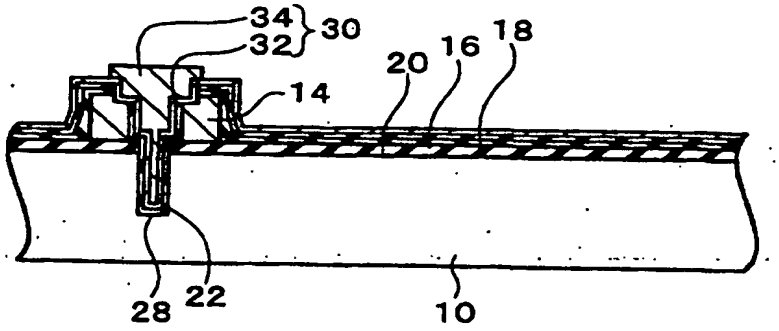


FIG. 2 C

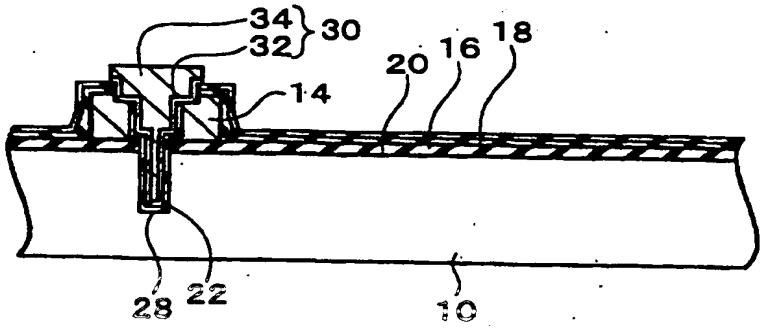


FIG. 2 D

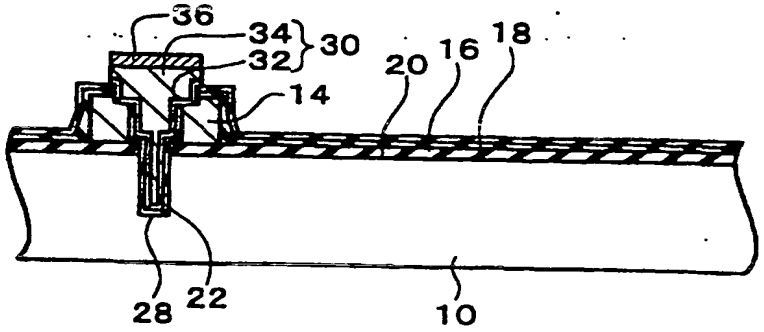


FIG. 3 A

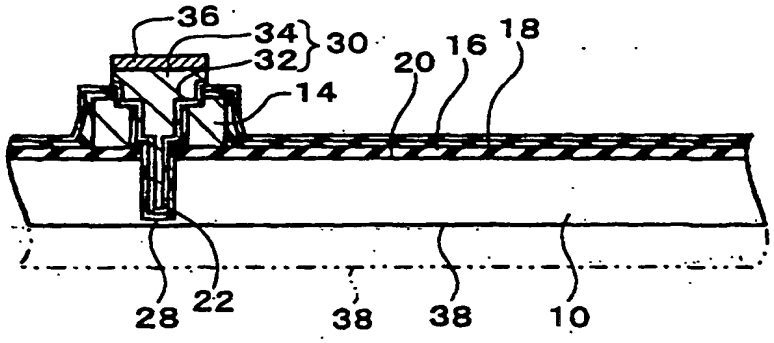


FIG. 3 B

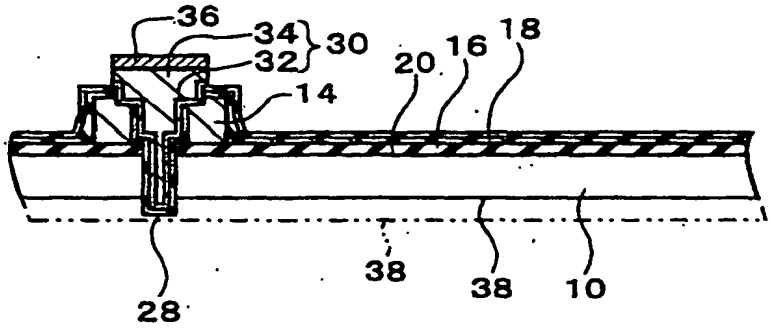


FIG. 3 C

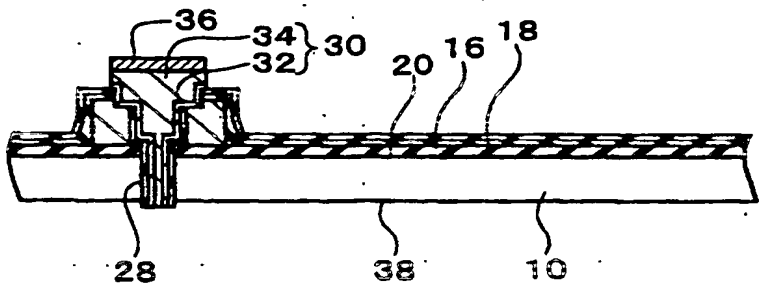


FIG. 4

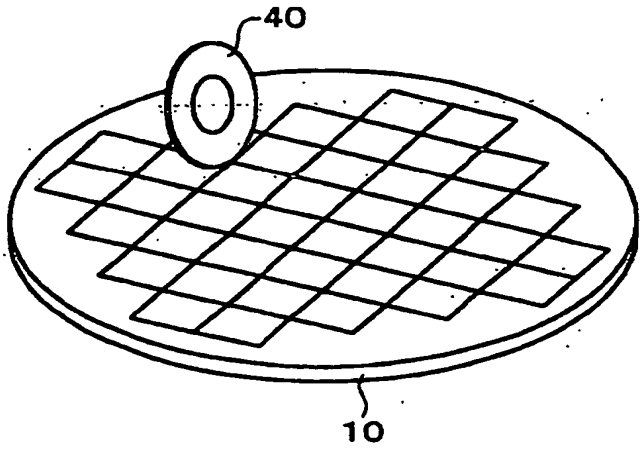


FIG. 5

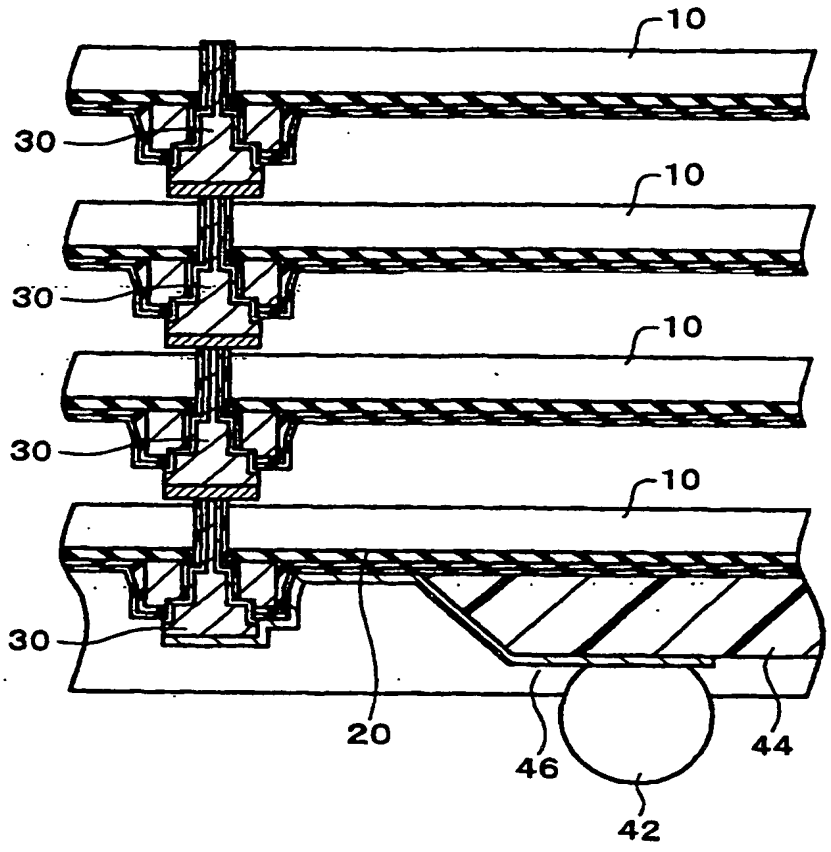


FIG. 6

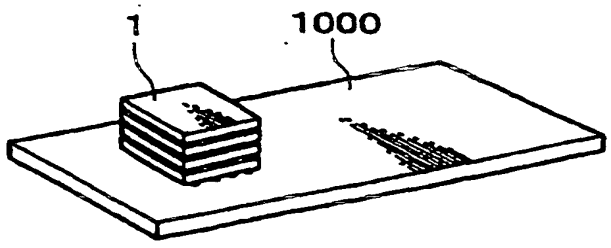


FIG. 7

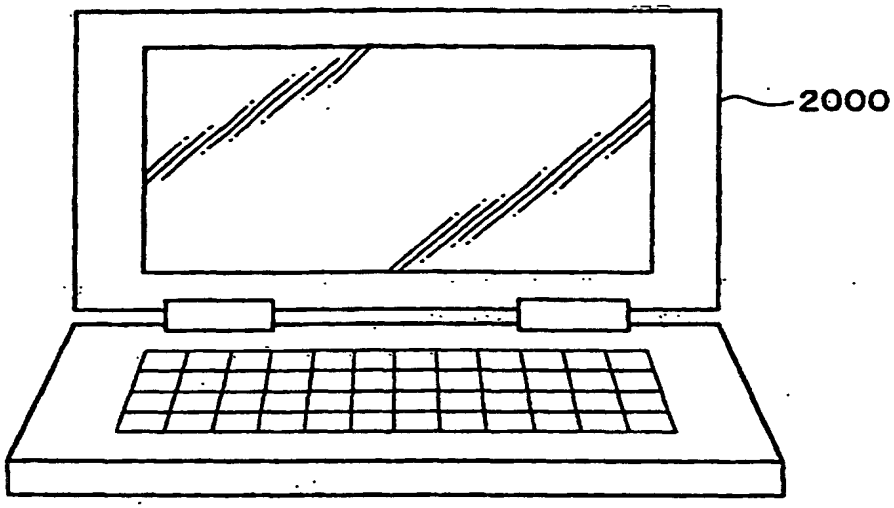


FIG. 8

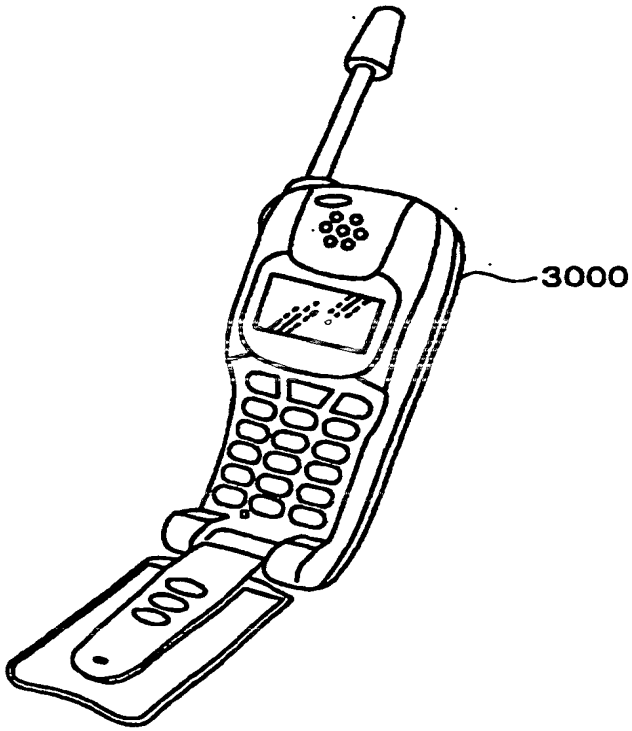


FIG. 9 A

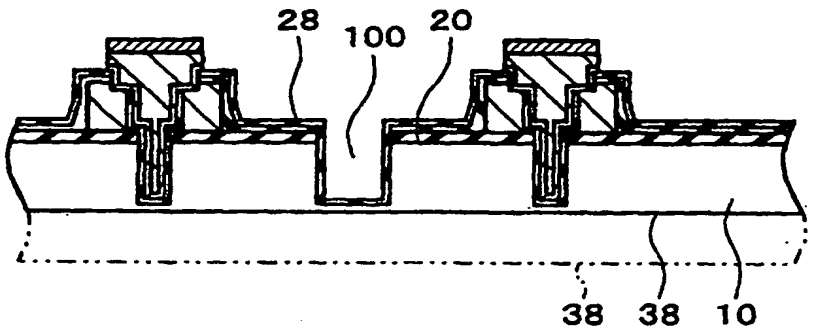


FIG. 9 B

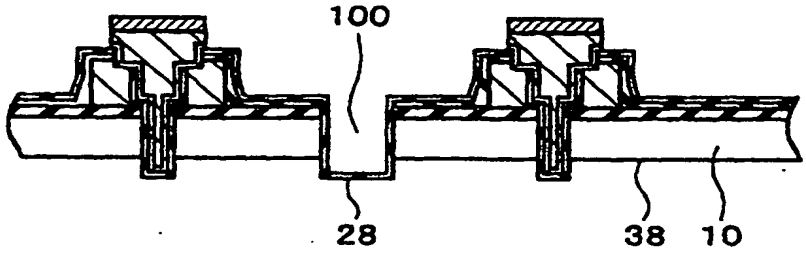


FIG. 9 C

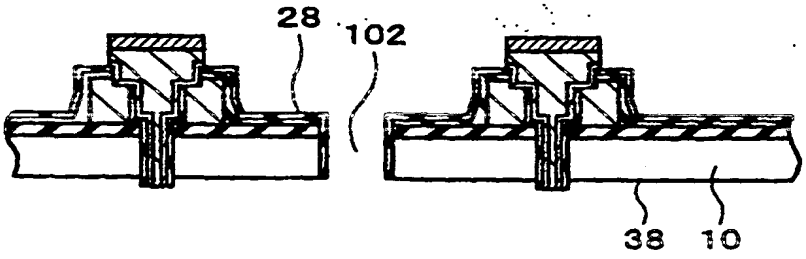


FIG. 10 A

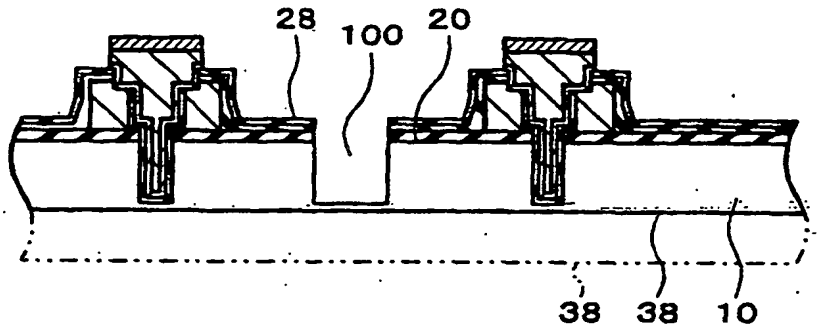


FIG. 10 B

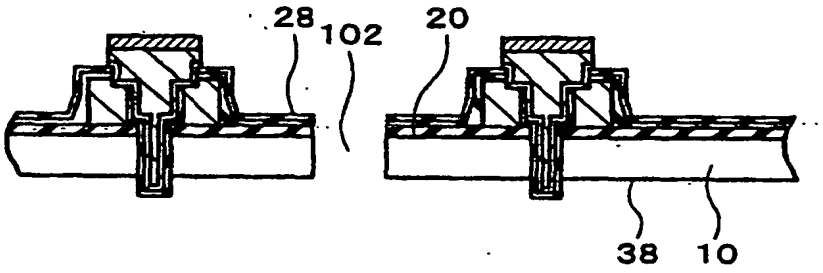


FIG. 11 A

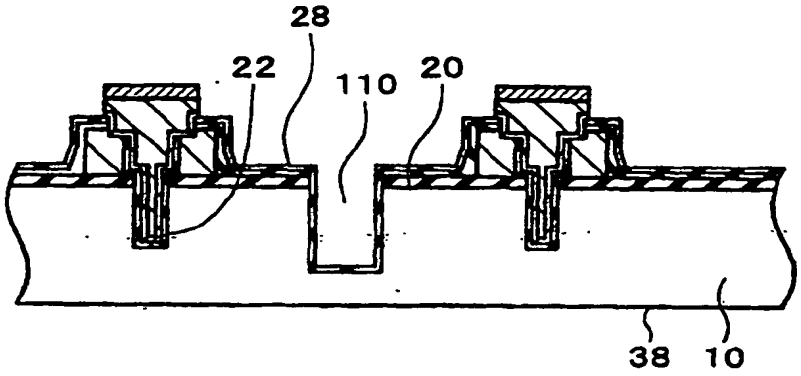


FIG. 11 B

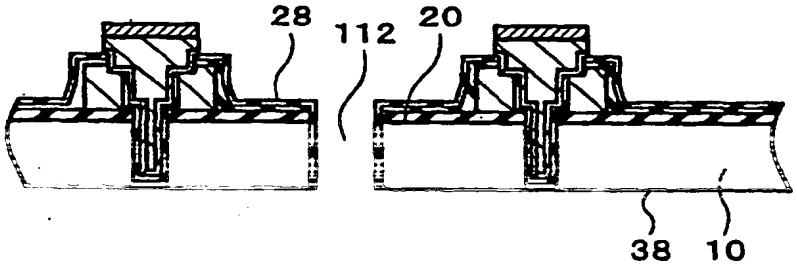


FIG. 12

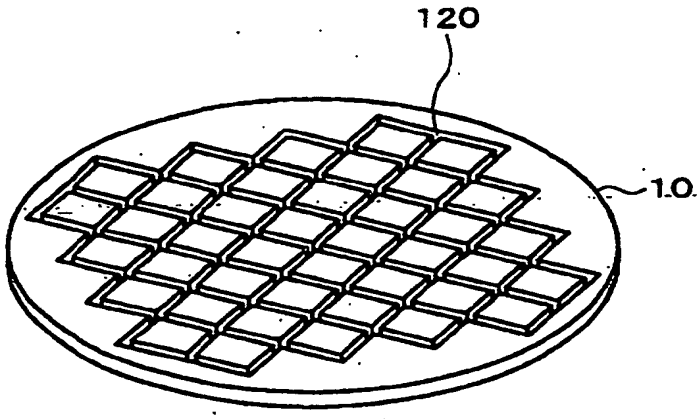
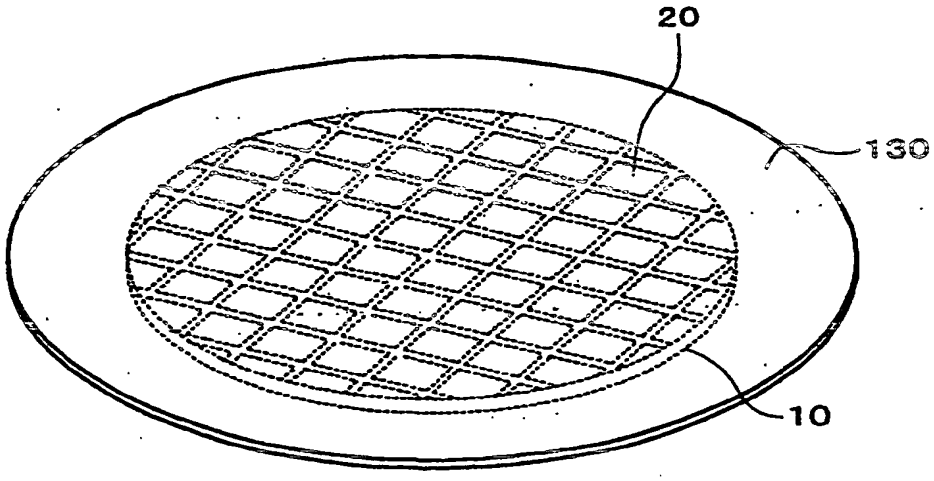


FIG. 13



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/03302

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L21/768, H01L25/065, H01L27/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L21/768, H01L25/065, H01L27/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2003
Kokai Jitsuyo Shinan Koho	1971-2003	Toroku Jitsuyo Shinan Koho	1994-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	JP 60-7148 A (NEC Corp.), 14 January, 1985 (14.01.85), Full text; Figs. 1 to 9 (Family: none)	1,4,7,8,13, 14,27-33 2,3,5,6, 9-12,15-26
X Y	JP 60-7149 A (NEC Corp.), 14 January, 1985 (14.01.85), Full text; Figs. 1 to 9 (Family: none)	1,4,7,8,13, 14,27-33 2,3,5,6, 9-12,15-26

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 June, 2003 (19.06.03)	01 July, 2003 (01.07.03)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/03302

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 98/19337 A1 (TRUSI TECHNOLOGIES, LLC), 07 May, 1998 (07.05.98), Full text; Figs. 1 to 18 & JP 2000-510288 A Full text; Figs. 1 to 18 & EP 948808 A1 & US 2002/0013061 A1 & US 2002/0063311 A1 & US 2002/0084513 A1 & US 2002/0127868 A1	1-14,27-33
Y	JP 2001-326325 A (Seiko Epson Corp.), 22 November, 2001 (22.11.01), Full text; Figs. 1 to 5 (Family: none)	1-33
Y	JP 2001-53218 A (Toshiba Corp.), 23 February, 2001 (23.02.01), Full text; Figs. 1 to 4 (Family: none)	1-33
A	US 5767001 A (SIEMENS AG.), 16 June, 1998 (16.06.98), Full text; Figs. 1 to 8 & JP 8-510360 A Full text; Figs. 1 to 8 & EP 698288 A1 & WO 94/25981 A1	1-33

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